A Ku-Band Ultra Super Low-noise Pseudomorphic Heterojunction FET in a Hollow Plastic PKG

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Abstract

This paper reports Ku-band ultra super low-noise pseudomorphic heterojunction FETs (pHJFETs) in a newly developed hollow plastic package. To achieve higher performance of pHJFETs, we employed further optimized epi-layer structure with good interfacial quality. The developed packaged HJFETs with 0.17 um T-shaped gate exhibited extremely low noise performance of 0.35 dB typical noise figure with 12.5 dB associated gain at 12 GHz.

I Introduction

Over the past several years, low noise performance of pHJFETs has been drastically improved[1-3]. To make further improvement in RF performance, HJFETs have been fabricated with shorter gate length. In accordance with increasing demand for very short gate length fabrication, it is inevitable to employ further optimized epi-layer structure with good interfacial quality.

To get the larger conduction-band discontinuities in the channel, several efforts have been made to increase the In composition of the channel[4-5]. As the segregation effects of In atoms during growth by molecular-beam epitaxy (MBE) cause composition gradation at the AlGaAs/InGaAs interface, several modified growth conditions have been proposed to improve the compositional abruptness of interfaces with InGaAs[6-7]. Recently, the dependence of pHJFET performances on In content with depth have been investigated. It is suggested that the performance of pHJFETs is most enhanced by a relatively high In content near the bottom of the quantum well[8].

In this paper, we report super low-noise pHJFETs with a sharp interfacial atomic profile AlGaAs/InGaAs epi-layer grown by MBE under the optimized growth conditions. The devices have a T-shaped gate with a very short footprint length (0.17 um), and exhibited typical noise figure of 0.35 dB with 12.5 dB associated gain at 12 GHz. Furthermore, a hollow plastic package has been newly developed, and has been shown to be effective in achieving high performance as well as low cost.

II Device Fabrication

The epi-layers were grown by MBE on (100) 3-inch semi -insulating GaAs substrates. The FET layers consist of i-GaAs buffer layer, 15 nm i-InGaAs channel layer, 40 nm donor AlGaAs layer with a density of 2×10^{18} cm^{-3} and 80 nm cap GaAs layer with a density of 3×10^{18} cm^{-3}. To improve the abruptness of the AlGaAs/InGaAs interface, we have successfully reduced In surface segregation using low substrate temperature and thermal desorption of the excess In during a growth interruption at the end of the InGaAs layer [9][10]. For comparison, the epi-layers without a growth interruption (non-optimized epi-layers) have also been prepared. SIMS depth profile for the improved AlGaAs/InGaAs epi-layer is shown in Fig. 1. The results indicate that In surface segregation at the AlGaAs/InGaAs interface is effectively suppressed. The measured sheet carrier concentration and the electron Hall mobility of the epitaxial wafers for the developed HJFETs are given in Table 1. The electron mobility obtained for the optimized channel layer is 25,000 $cm^2v^{-1}s^{-1}$ at 77 k, which is much higher

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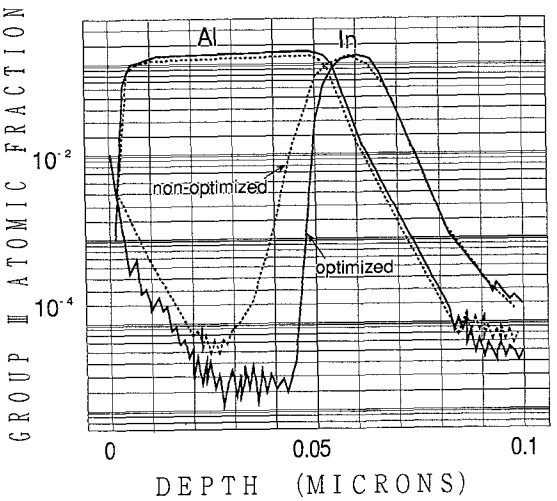

Fig.1 The results of SIMS In, Al depth profiling analysis.

Table 1 The measured the electron Hall mobility and sheet carrier concentration data at 77K.

channel	electron Hall mobility($cm^2v^{-1}s^{-1}$)	sheet carrier concentration (cm^{-2})
optimized channel layer	25,000	1.6×10^{12}
non-optimized channel layer	13,000	2.0×10^{12}

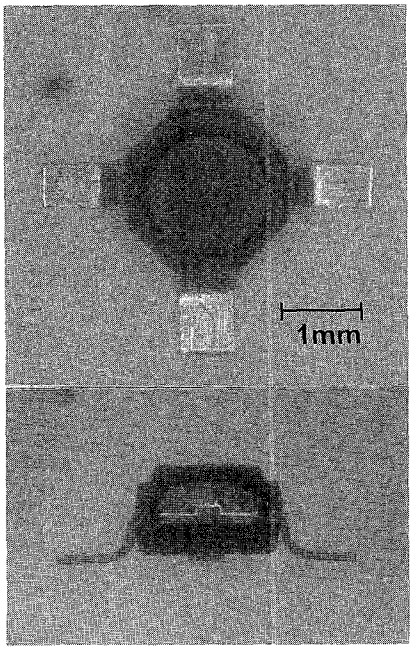

Fig.2 Tope and cross-sectional view of a developed hollow plastic package.

than that obtained for the non-optimized channel layer.

The developed HJFETs have 4 gate fingers. T-shaped gates were fabricated by electron-beam evaporation and a lift-off technique employing direct-write electron-beam lithography [11]. The gate length and the total gate width are 0.17 um and 200 um, respectively. The 4-finger gate device has the airbridged-drain structure to reduce the parasitic gate-source capacitance.

The HJFETs were assembled in plastic packages with a hallow structure, which has been newly developed for use in high frequency application. The cross section of the new hollow plastic package is shown Fig. 2. The plastic package consists of the lead frame embedded on the surface of the plastic platform, the bank on the outside of plastic platform to get enough lead strength and the plastic cap adhered on the bank so as to seal the chip in the package. The plastic package size is 2 mm across, 1.45 mm thick and 4 mm long containing the lead-length.

Ⅲ Device Performance

Figure 3 shows gate bias dependence of the measured transcondutance for the optimized channel HJFET's at a drain voltage of 2.0 V. The device exhibits a peak transconductance of 535 mS/mm and good pinch-off characteristics. The results for the non-optimized channel devices are also plotted in Fig. 3. A 10 percent improvement in extrinsic gm is obtained for the optimized channel HJFET. The superior gm characteristics are considered to be due to the mobility improvement in electron transport properties for the effective prevention of the In segregation at the AlGaAs/InGaAs interface.

On-wafer device S-parameter measurements have been performed in the frequency range from 50 MHz to 40 GHz by using a Cascade Microtech microwave probe station and Wiltron360 network analyzer. The cut-off frequency f_T as a function of drain current for the devices , obtained by extrapolating the current gain H21 at -6 dB/octave, are shown Fig.4. The device with the optimized channel shows higher cut-off frequencies than those for the non-optimized channel device over the whole drain current range investigated.

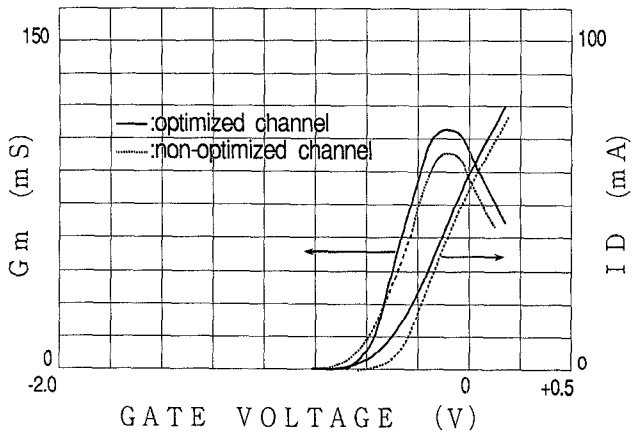

Fig.3 The transconductance gm and the drain current I_D as a function of the gate voltage measured at a drain voltage V_D of 2.0V.

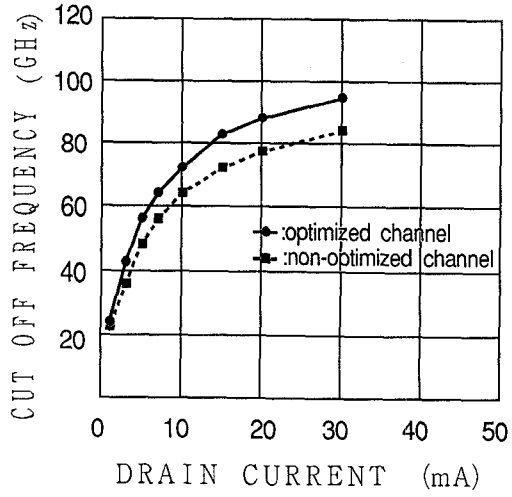

Fig.4 The cut-off frequency f_T as a junction of drain current for the devices at a drain voltage V_D of 2.0V.

The noise performance for the plastic packaged HJFETs was evaluated at 12 GHz. The drain current dependence of the noise figure and the associated gain at 12 GHz are shown in Fig. 5. The minimum noise figure of 0.31 dB with the associated gain of 12.9 dB was obtained at a drain current of 12 mA. Fig. 6 shows the distribution of noise figure and associated gain at 12 GHz at 2 V drain voltage and 10 mA drain current. The average noise figure is 0.35 dB with the average associated gain of 12.5 dB. These RF characteristics for the HJFET's in the plastic packages are almost the same as those for the HJFET's in conventional ceramic packages.

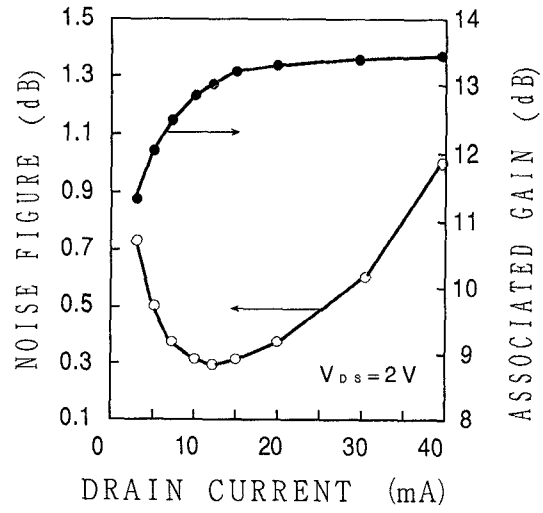

Fig.5 The drain current dependences of the noise figure and associated gain at 12GHz.

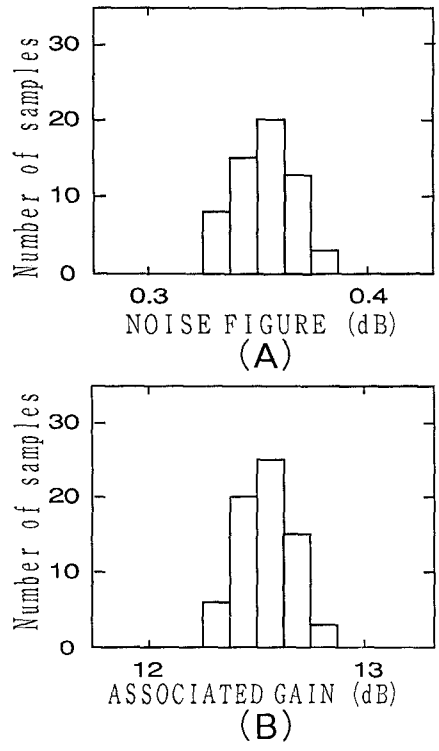

Fig.6 Distribution of noise figure (A) and associated gain (B) at a drain current I_D of 10mA and drain voltage V_D of 2.0V.

The equivalent circuit parameters of the packaged HJFETs are summarized in Table 2. The device was biased at a drain voltage of 2 V and a drain current of 10 mA. The parasitic capacitance between the gate and ground lead was obtained of 0.03 pF, which is enough small compared to conventional transfer molded plastic packages.

Table 2 The equivalent circuit parameters for the packaged HJFET obtained by S-parameter measurements.

Parameter (chip)	Value
gm	75mS
gd	5.9mS
Cgs	0.15pF
Cdg	0.03pF
Cds	0.07pF
Ri	4Ω
Rs	1.9Ω
Rd	2.1Ω
Rg	1.0Ω

Parameter (package)	Value
Lg	0.29nH
Ld	0.48nH
Ls	0.06nH
Cg	0.03pF
Cd	0.05pF
Rg	0.065Ω
Rd	0.065Ω

Ⅳ Conclusion

Super-low noise HJFET's with an optimized epi-layer structure has been newly developed. The developed HJFET's showed higher cut-off frequencies compared to non-optimized channel FET. Extremely low noise performance has been achieved for the newly developed plastic packaged pseudomorphic HJFETs with 0.17 um T-shaped gate. Typical noise figure of 0.35 dB with 12.5 dB associated gain has been obtained at 12 GHz. These HJFETs in the plastic package are promising for future wide application area.

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